Fly-Over: A Light-Weight Distributed Power-Gating Mechanism for Energy-Efficient Networks-on-Chip

Rahul Boyapati*, Jiayi Huang*, Ningyuan Wang†, Kyung Hoon Kim, Ki Hwan Yum, Eun Jung Kim
Department of Computer Science and Engineering, Texas A&M University, USA  †Google Inc.

Introduction

- Networks-on-Chip (NoCs) are devouring a large fraction of the on-chip power budget as technology scales down.
- In addition, static NoC power consumption is becoming the dominant component.
- **Fly-Over (FLOV):** a lightweight distributed router power-gating mechanism to reduce NoC static power consumption.
  - FLOV router: FLOV links for network connectivity and low-latency route over power-gated routers.
  - Handshake Protocol: allows for seamless power-gating between neighboring routers.
  - Dynamic Routing Algorithm: best-effort minimal path routing without knowledge of global network status.

FLOV Router Microarchitecture

- **ON (Active/Draining) mode:** Packets are directed through the baseline router.
- **GATED (Sleep/Wakeup) mode:** Baseline router portion is power gated/waking up, packets fly over the baseline router through FLOV links.

Handshake Protocol

- Handshake Controller: handshaking with neighbors to facilitate power-gating/wakeup.
- Power State Register (PSRs): keeps the power state of physical/logical neighbor routers.
- Credit Control Logic, Augmented to relay credits while router core is gated.

Dynamic Routing Algorithm

- Partition-based dynamic routing algorithm based on YX routing — best effort minimal routing.
- The right-most column always-active routers maintains network connectivity with FLOV links.

Evaluation Methodology & Results

- Simulation Testbed Parameters
  - Network Topology: 8x8 Mesh
  - Router: 3-stage (3 cycles) router
  - Virtual Channel: 3 regular VCs and 1 escape VC per vnet, 3 vnets, 6-flit depth
  - Packet Size: 4 flits/packet for synthetic workload
  - Memory Hierarchy: 32KB L1 DS, 8MB L2S, MESI, 4 MCs at 4 corners
  - Technology: 32 nm
  - Clock Frequency: 2 GHz
  - Link: 1 mm, 1 cycle, 168 width
  - Power-Gating Overhead = 17.7 flits, Wakeup latency = 10 cycles
  - Baseline Routing: YX routing

- PARSEC Benchmarks Evaluation
  - Static Energy
  - Dynamic Energy

- Network Reconfiguration Overhead
  - FLOV power-gating is light-weight in terms of latency, while RP’s centralized power gating control incurs high network latency, reconfiguration phase I is more than 700 cycles.

- Reference: