To be submitted online:

1. All logisim or Y86 files developed
2. Individual one-page reports per team-member (similar to what you submitted for Lab-4)
3. Names of all your team-members with their corresponding sections

* For Activity 1
("Design a minimal instruction set architecture for an 8 bit load-store processor with appropriate binary encoding. Describe the ISA in detail in the report with all your design assumptions and rationale.")

1. Detailed description of your Instruction Set Architecture covering the following points
   a. A table showing the all the instructions you implemented, along with their op-codes.
   b. For each instruction, explain what the instruction does along with the format of the instruction in terms of bit width – such as which bits represent the op-codes, which bits represent the values being read in (if applicable).

* For Activity 2
("create a program to perform the matrix addition.")

Attach your Y86 assembly code, and corresponding captured output screen (generated by YIS). Clearly mention your assumption for matrix A, matrix B, and expected output matrix C.

* For Activity 3
("Design and verify a minimal processor that can execute the ISA designed in activity # 1. Only design the bare minimum circuits which are absolutely essential to execute the program that you created in assembly.")

1. For each functional block of the processor.
   a. Explain its operation. (You may want to insert screen shots from Logisim to help you in your explanation)
   b. If you split the work of creating these various sub-blocks, clearly demarcate which parts were contributed by each of the members.

* For Activity 4
Show your demo to TA, it’s part of the grading.